

FIG. 1 (Prior Art)

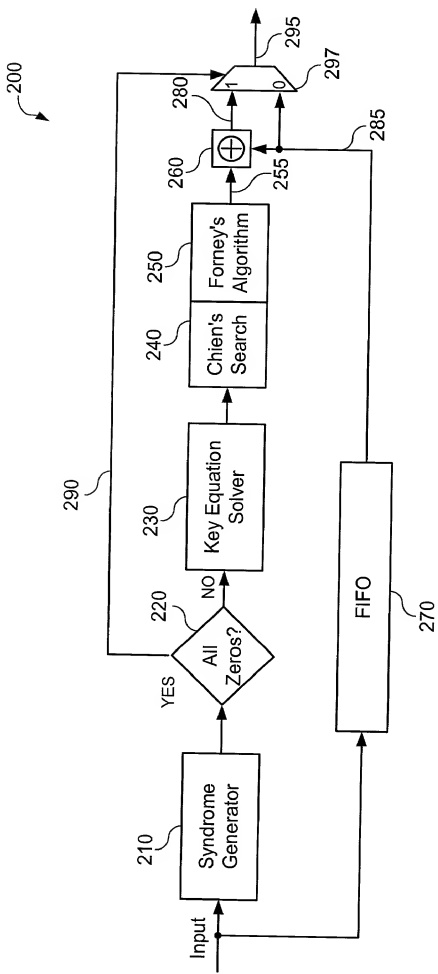


FIG. 2 (Prior Art)

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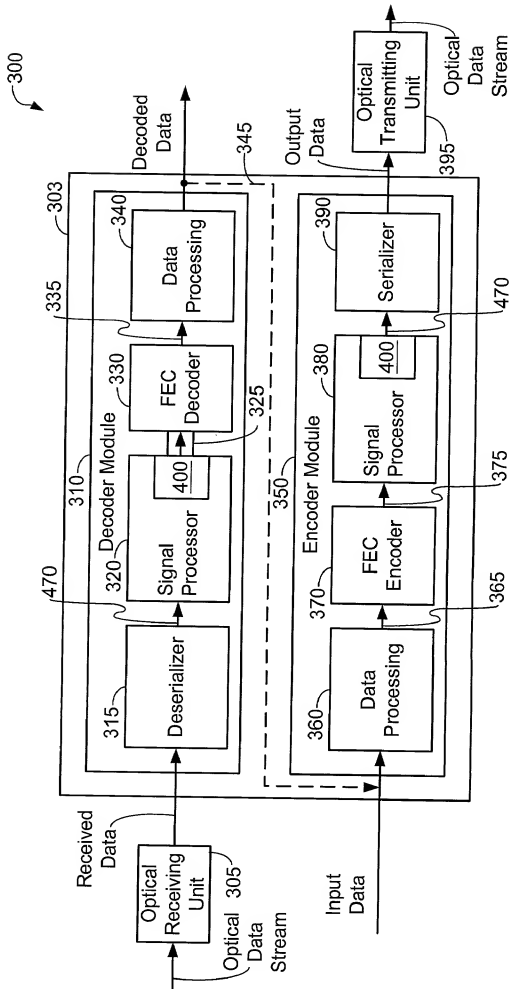


FIG. 3

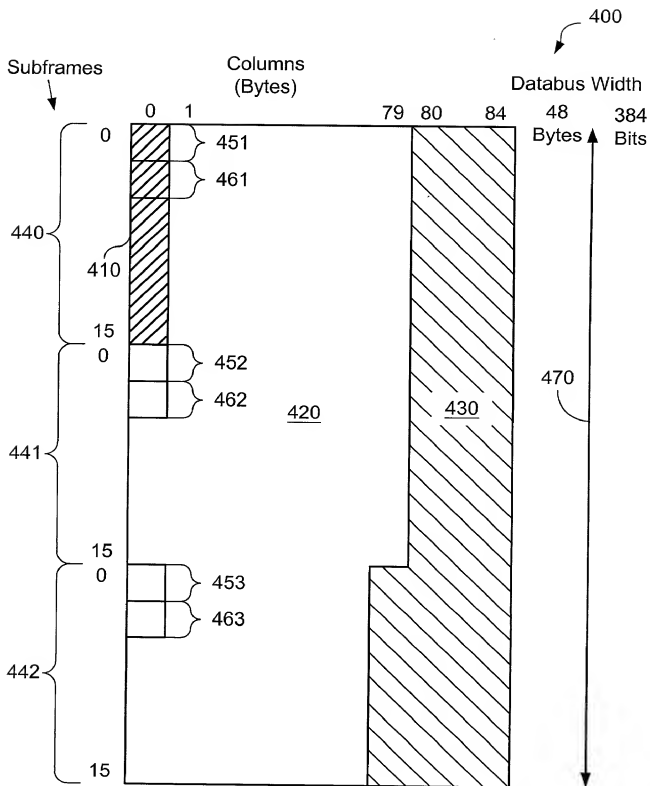


FIG. 4

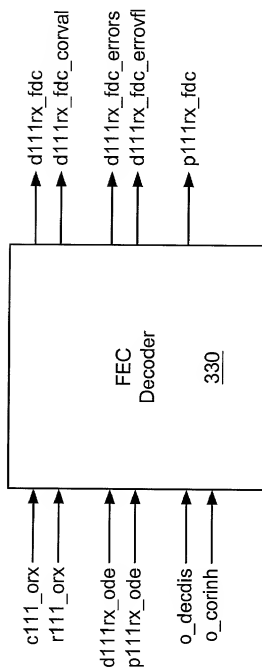


FIG. 5

Name	Direction	Width	Description
c111_orx	IN	std_ulogic	System clock, 111 MHz
r111_orx	IN	std_ulogic	Signal for synchronous reset of decoder
d111rx_ode	IN	(383 down to 0)	Input encoded data
p111rx_ode	IN	std_ulogic	Start of input FEC block pulse
o_decdis	IN	std_ulogic	Decoder function enable ('1' = decoder is disabled)
o_corinh	IN	std_ulogic	Error correction enable ('1' = error correction inhibited)
d111rx_fdc	BUFFER	(383 down to 0)	Output decoded data
d111rx_fdc_corval	BUFFER	(383 down to 0)	Output correction values: This signal indicates the bit position in the data stream d111rx_fdc where a bit has been corrected (values: '0' = no correction; '1' = correction)
p111rx_fdc	BUFFER	std_ulogic	Pulse indicating the start of an output FEC block
d111rx_fdc_errors	BUFFER	(10 down to 0)	Number of corrected bit errors within one frame
d111rx_fdc_errorfl	BUFFER	(4 down to 0)	Number of uncorrectable blocks within one frame

FIG. 6

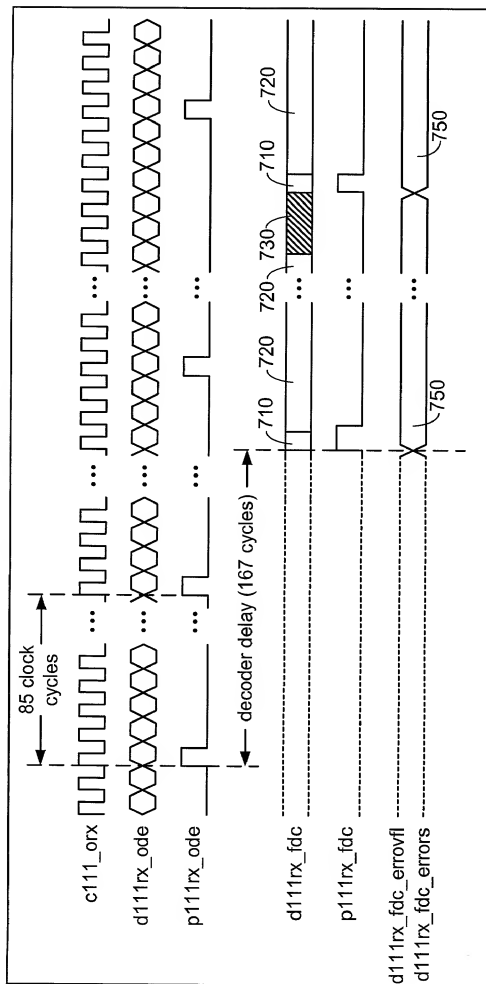


FIG. 7

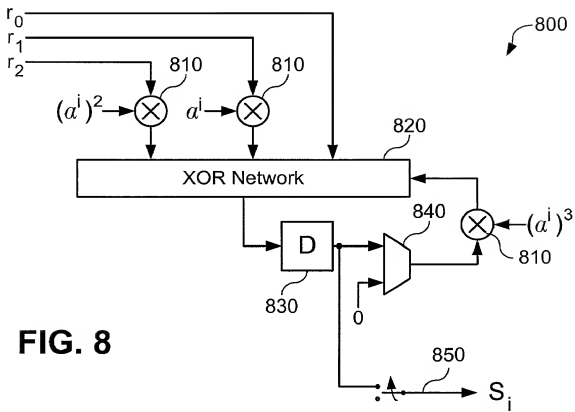
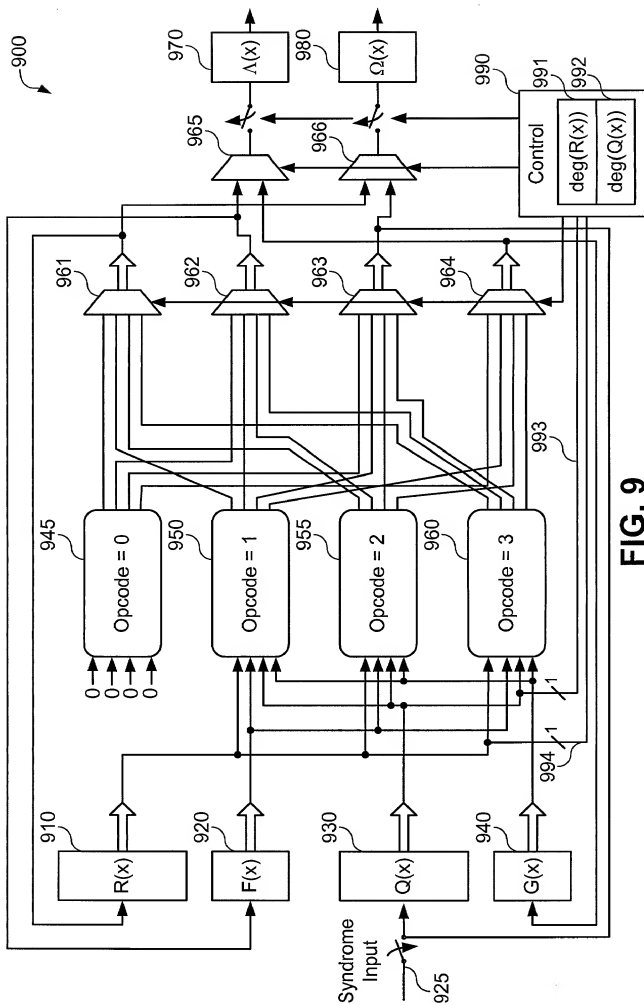


FIG. 8

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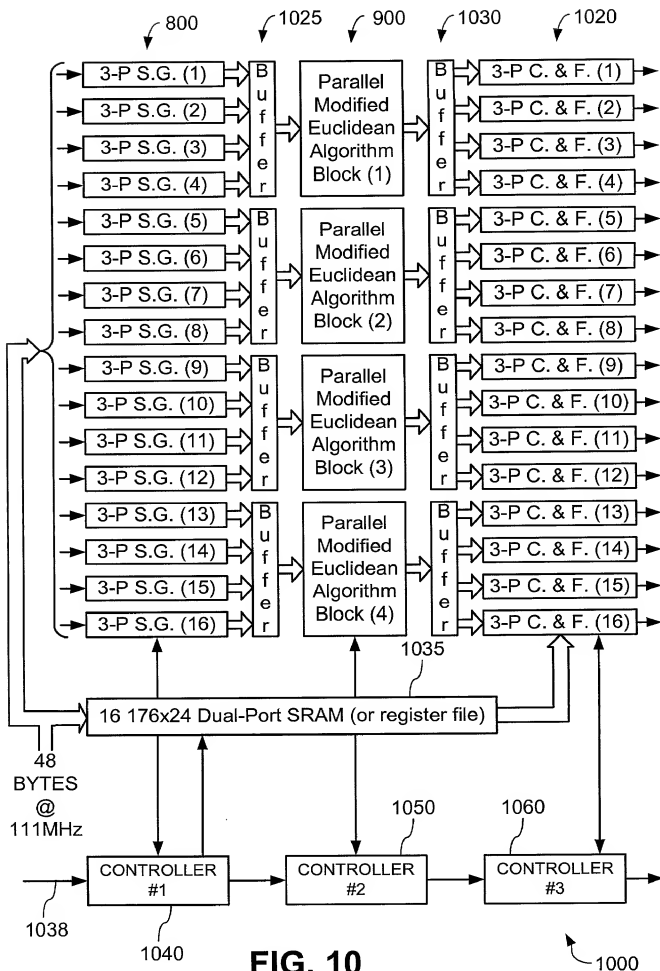


FIG. 10

FIG. 11

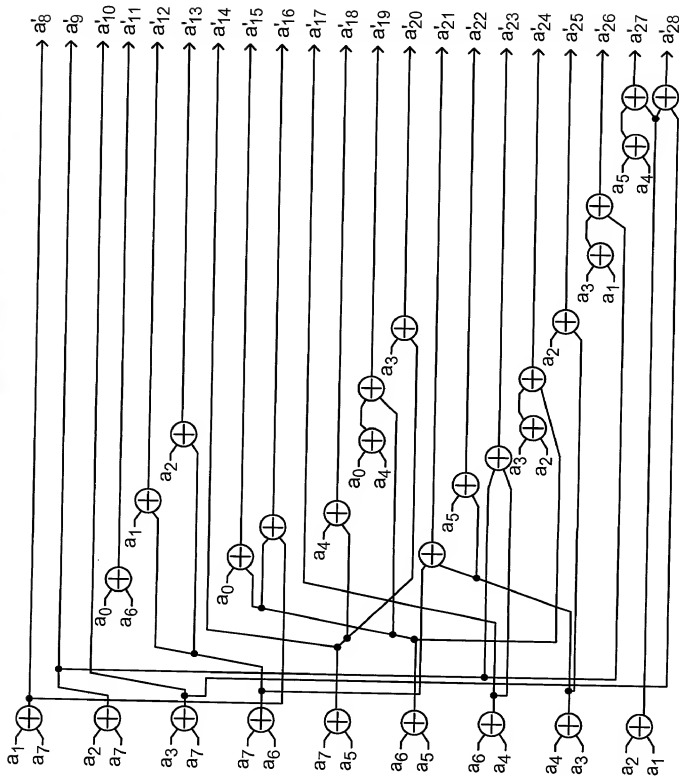


FIG. 11

1100

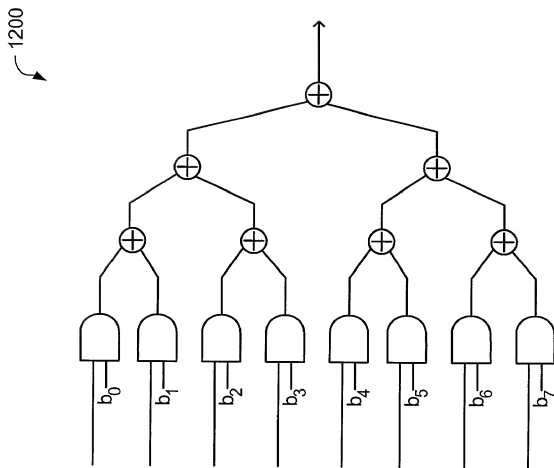


FIG. 12

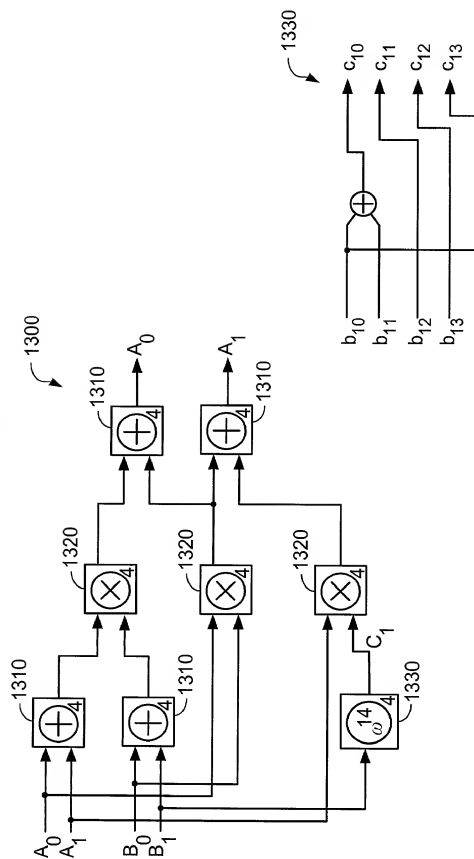


FIG. 13A

FIG. 13B

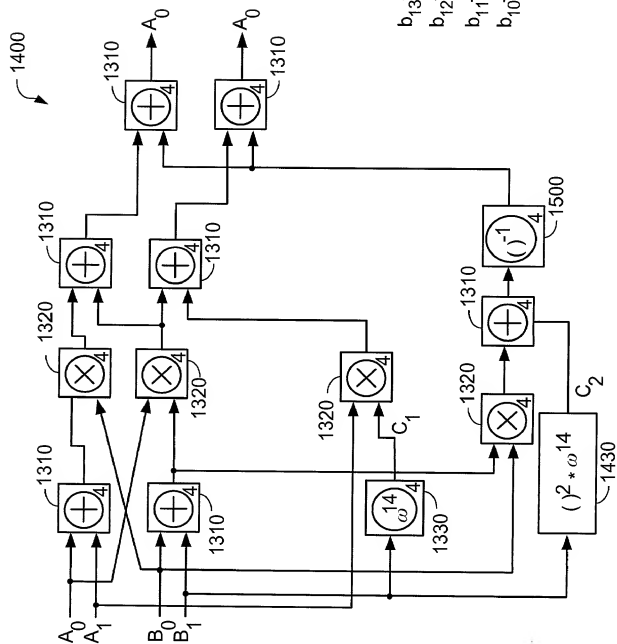


FIG. 14A

FIG. 14B

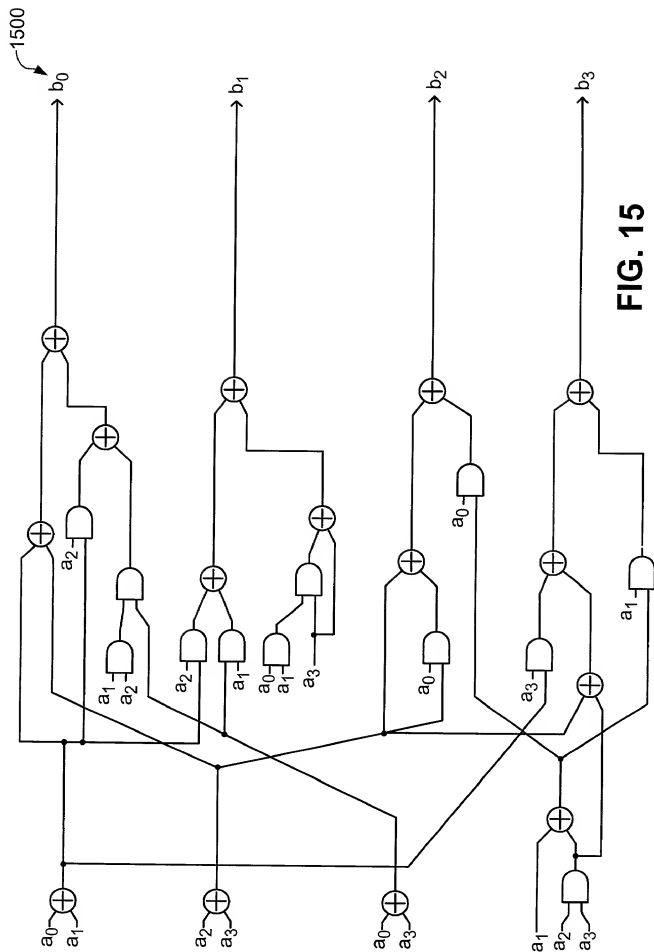


FIG. 15

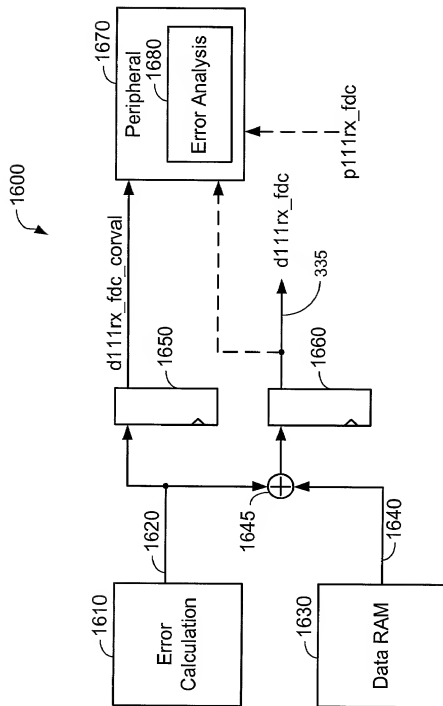


FIG. 16

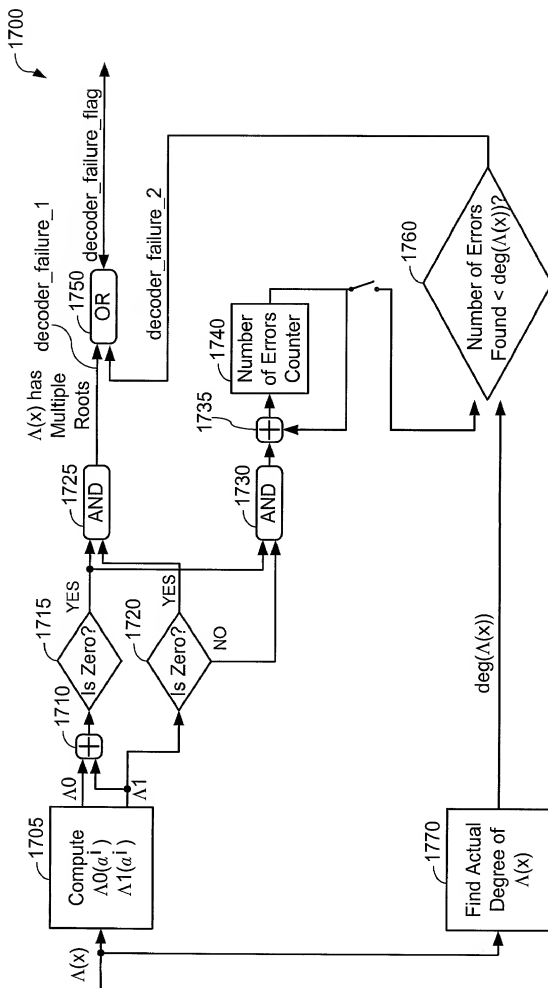


FIG. 17

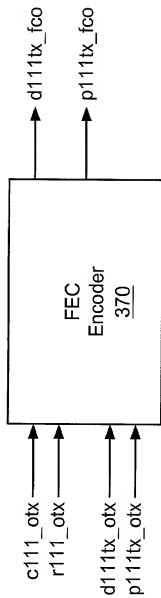


FIG. 18

Name	Direction	Width	Description
c111_otx	IN	std_ulogic	System clock, 111 MHz
r111_otx	IN	std_ulogic	Signal for synchronous reset of encoder
d111tx_otx	IN	(383 down to 0)	Input data
p111tx_otx	IN	std_ulogic	Start of input FEC block pulse
d111tx_fco	BUFFER	(383 down to 0)	Output encoded data
p111tx_fco	BUFFER	std_ulogic	Pulse indicating the end of an FEC block

FIG. 19

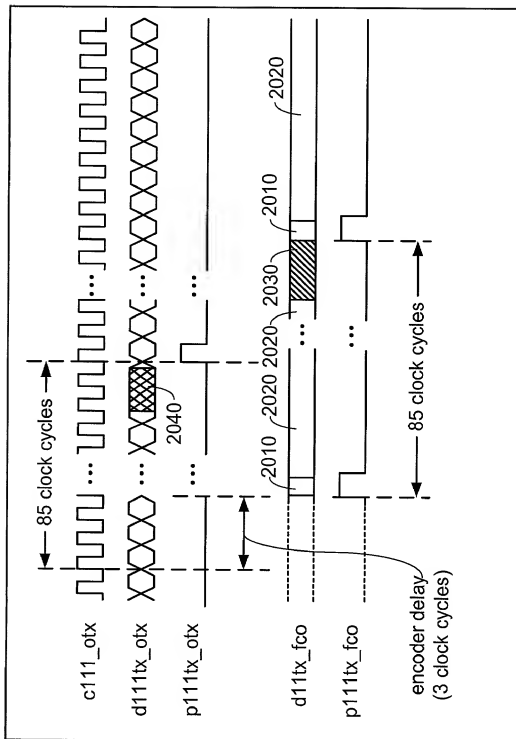
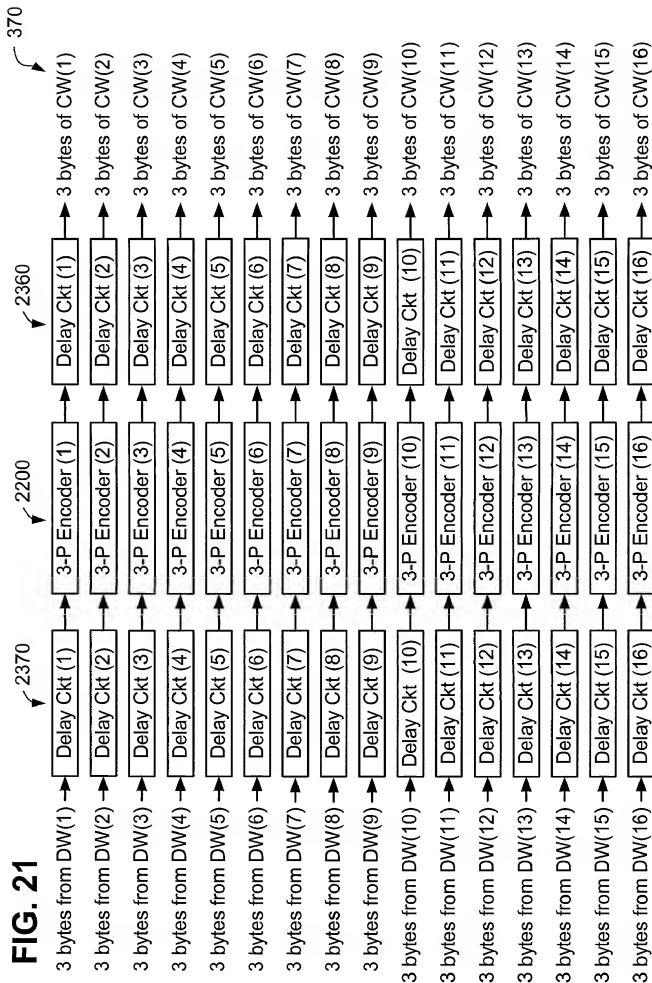


FIG. 20

FIG. 21



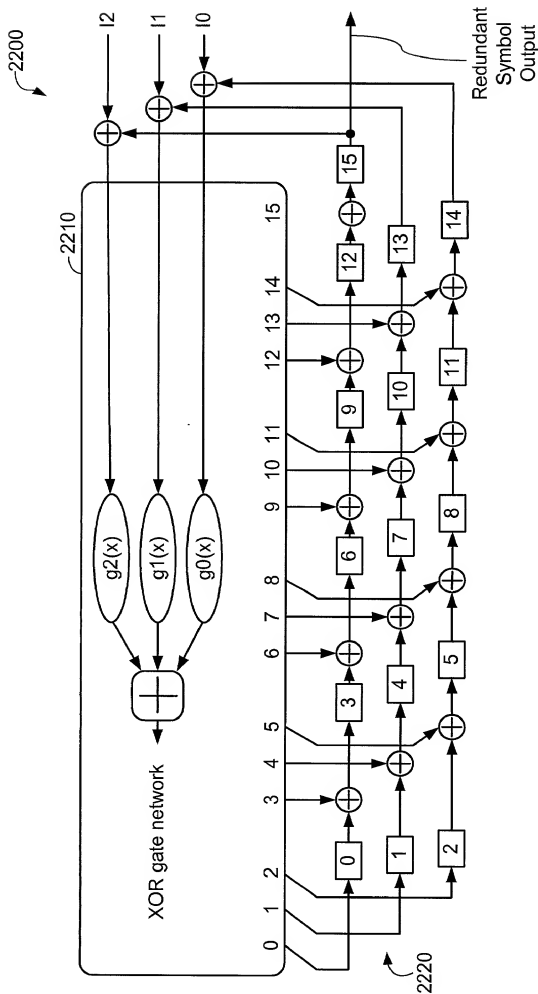


FIG. 22

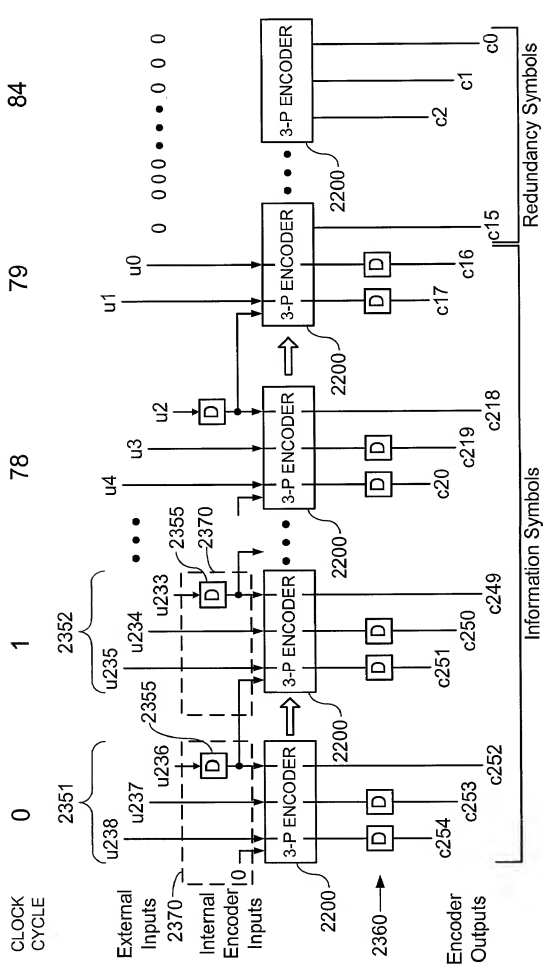


FIG. 23